



SWARNANDHRA

COLLEGE OF ENGINEERING & TECHNOLOGY

Accredited by National Board of Accreditation.
 AICTE, New Delhi, Accredited by NAAC with "A" Grade - 3.32 CGPA
 Recognized under 2(f) & 12(B) of UGC Act 1956, Approved by AICTE, New Delhi.
 Permanent Affiliation to JNTUK, Kakinada
 SEETHARAMPURAM, W.G.D.T., NARSAPUR-534280, (Andhra Pradesh)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

TEACHING PLAN

Course Code	Course Title	Semester	Branch	Contact Period /Week	Academic Year	Semester commencement date
19EC5T01	Linear & Digital IC Applications (R19)	V	ECE	5	2021-22	04-10-2021

COURSE OUTCOMES

After completion of the course student are able to

1	Demonstrate different applications based on operational-amplifier.(K1,K2,K3)
2	Explain the applications of waveform generators based on operational-amplifier and IC 555 timer.(K1,K2,K4)
3	Sketch and implementation of Combinational circuits using digital ICs.(K3)
4	Sketch and implementation of Sequential circuits using digital ICs (K3)

Unit No	OutCome/ Bloom's Level	Topics/Activity	Reference Text book	Contact Periods	Delivery Method	
1.	CO1: Demonstrate different applications based on operational-amplifier.(K1,K2,K3)	1. INTEGRATED CIRCUITS				Chalk & Talk, PPT, Active Learning & Tutorial
		1.1	Introduction, Integrated circuits- Types, Classification	T1, T2	1	
		1.2	Package Types and temperature ranges.	T1, T2	1	
		1.3	Differential Amplifier- DC and AC analysis of Dual input balanced output Configuration	T1, T2	1	
		1.4	Properties of other differential amplifier configuration (Dual Input Unbalanced Output, Single Ended Input - Balanced/ Unbalanced Output)	T1, T2	1	
		1.5	Properties of other differential amplifier configuration (Dual Input Single Ended Input)	T1, T2	1	
		1.6	Properties of other differential amplifier configuration (Balanced/ Unbalanced Output)	T1, T2	1	
		1.7	DC Coupling.	T1, T2	1	



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	1.8	Cascade Differential Amplifier Stages,	T1, T2	1	
	1.9	Level translator	T1, T2	1	
	1.10	Problems	T1, T2	1	
TOTAL				10	
2.	2. OPERATIONAL AMPLIFIER AND ITS APPLICATIONS				
	2.1	Characteristics of OP-Amps, Op-amp Block Diagram	T1, T2	1	Chalk & Talk, PPT, Active Learning & Tutorial
	2.2	Ideal and practical Op-amp specifications. Op-Amp parameters, (DC characteristics)	T1, T2	1	
	2.3	Ideal and practical Op-amp specifications. Op-Amp parameters, (AC characteristics)	T1, T2	1	
	2.4	741 op-amp & its features	T1, T2	1	
	2.5	Linear Applications of Op-Amps: Inverting amplifier	T1, T2	1	
	2.6	Linear Applications of Op-Amps: Non-inverting amplifier	T1, T2	1	
	2.7	Integrator and differentiator	T1, T2	1	
	2.8	Summing and Difference amplifier	T1, T2	1	
	2.9	Non-Linear Applications of Op-Amps: Comparators	T1, T2	1	
	2.10	Triangular and Square wave generators	T1, T2	1	
	2.11	Sine wave generation: principle, Wein-bridge	T1, T2	1	
	2.12	Phase-shift oscillators. and Problems	T1, T2	1	
TOTAL				10	
3.	3. ACTIVE FILTERS AND TIMERS				
	3.1	Introduction, classification, Butter worth filters – 1st order LPF	T1, T2	1	Chalk & Talk, PPT, Active Learning & Case study
	3.2	Butter worth filters – 1st order HPF	T1, T2	1	
	3.3	Band pass, Band reject	T1, T2	1	
	3.4	All pass filters qualitative and quantitative analysis	T1, T2	1	
	3.5	Introduction to 555 timer	T1, T2	1	
	3.6	555 timer, functional diagram	T1, T2	1	
	3.7	Monostable operations and applications	T2, T2	1	



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	3.8	Astable operations and applications	T1,T2	1	
	3.9	Schmitt Trigger,PLL(IC 565)	T1,T2	1	
	3.10	VCO(IC 566),Problems	T1,T2	1	
	TOTAL			10	
4.	4. COMBINATIONAL LOGIC DESIGN				Chalk & Talk,PPT, Active Learning & Project based learning
	4.1	Introduction, Design and Analysis procedures,	T3	1	
	4.2	Decoders ,Encoders,	T3	1	
	4.3	Multiplexers and de-multiplexers,	T3	1	
	4.4	Comparators	T3	1	
	4.5	Ripple Adder	T3	1	
	4.6	Binary Parallel Adder	T3	1	
	4.7	Binary Adder-Subtractor	T3	1	
	4.8	Combinational multipliers	T3	1	
	4.9	Design considerations of the above combinational circuits with relevant Digital ICs	T3	1	
	4.10	Combinational circuits with relevant Digital ICs	T3	1	
TOTAL			10		
5.	5. SEQUENTIAL LOGIC DESIGN				Chalk & Talk, PPT, Active Learning & Tutorial
	5.1	Introduction to SSI latches	T3	1	
	5.2	Flip-Flops: SR,JK	T3	1	
	5.3	D flipflop, T Flipflop	T3	1	
	5.4	Design of Counters using Digital ICs,	T3	1	
	5.5	Counter applications	T3	1	
	5.6	Synchronous design methodology	T3	1	
	5.7	Universal Shift Registers	T3	1	
	5.8	Ring Counter	T3	1	
	5.9	Johnson Counter	T3	1	
	5.10	Design considerations sequential logic circuits with relevant Digital ICs	T3	1	
	Additional topics	Log and Antilog amplifiers, Instrumentation amplifier and A to D coverters			
TOTAL			10		
TOTAL NO. OF CLASSES PROPOSED PER PERIOD'S				60	



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Text Books:

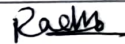
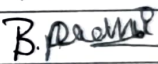

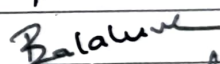
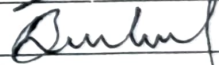
No.	AUTHORS/BOOK TITLE/EDITION(latest)/PUBLISHER/YEAR OF PUBLICATION
	D. Roy Chowdary, "Linear Integrated Circuits", 2 nd Edition, New Age International (p) Ltd, 2003. Unit-I, II, III.
	F. Wakerly, "Digital Design Principles & Practices", 3rd Edition, PHI/ Pearson Education Asia, 2005. Unit-IV, V

Reference Books:

No.	AUTHORS/BOOK TITLE/EDITION(latest)/PUBLISHER/YEAR OF PUBLICATION
	Sergio Franco, "Design with Operational Amplifiers & Analog Integrated Circuits", 1 st Edition, McGraw Hill, 1988. Unit-I, II, III.
	M. Morris Mano, "Digital Logic and Computer Design", 1 st Edition Pearson Education, 2016, Unit-IV, V

Website Details

www.nptel.ac.in
www.slideshare.net
https://youtu.be/Z-Hw3CpPVj0

	Name	Signature with Date
Faculty	Mrs. Radha Rani	
Faculty II(for common Course)	Mrs. B. Pavani	
i. Course Coordinator	Mrs. Radha Rani	
Module Coordinator	Dr.K.Balamurugan	
Programme Coordinator	Dr. B. S. Rao	


Principal